Mitigation of Single Event Upset Effects in Nanosheet FET 6T SRAM Cell

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Abstract

Advanced gate-all-around (GAA) nanosheet field-effect transistors (NSFETs) are promising for scaled static random-access memory (SRAM), but radiation-generated charge can disturb internal storage nodes and cause a single-event upset (SEU). This paper presents a structured analysis and reproducibility framework based on the 2024 IEEE Access study by Bang et al. on a 3-nm-node NSFET 6T SRAM cell. The source study used Sentaurus technology computer-aided design (TCAD) to examine alpha-particle and heavy-ion strikes, compare strike locations, and evaluate partial bottom dielectric isolation (PDI). It identifies the drain–channel junction of an off pull-down transistor as a sensitive region and reports that hold operation is the most vulnerable mode among those tested. Published results show that PDI reduces collected charge relative to a conventional structure for the evaluated heavy-ion linear energy transfer (LET) values. This draft organizes the problem, literature context, device physics, equations, simulation workflow, and selected comparative results into an IEEE-style manuscript. A follow-on study is proposed to sweep PDI geometry and strike conditions using calibrated TCAD models. Numerical values reproduced here are explicitly identified as published values; no new simulation or experimental results are claimed. The framework is intended to support a transparent investigation of SEU tolerance while accounting for trade-offs in device performance, process complexity, and radiation immunity.

Keywords

Gate-all-around (GAA), nanosheet FET (NSFET), static random-access memory (SRAM), single-event upset (SEU), linear energy transfer (LET), partial bottom dielectric isolation (PDI).

I. Introduction

Static random-access memory is widely used in processor caches, embedded systems, and high-speed data paths because it provides fast access without refresh. A conventional 6T SRAM bitcell stores one bit using two cross-coupled inverters and two access transistors. The cross-coupled inverters provide regenerative feedback, while the access devices connect the internal storage nodes to the bit lines under word-line control.

A single-event upset occurs when an energetic particle deposits charge near a sensitive semiconductor region. The resulting transient current can disturb a storage node. If the disturbance exceeds the restoring capability of the cross-coupled inverters, the stored logic state may reverse. The consequences range from corrupted data to system-level malfunction. SEU reliability is relevant to terrestrial electronics as well as

space, automotive, and safety-critical applications.

Gate-all-around nanosheet FETs provide strong electrostatic control and are considered for technology nodes beyond FinFET scaling. Their three-dimensional geometry and small dimensions nevertheless require radiation response to be evaluated rather than assumed. Bang et al. [1] studied a 3-nm-node NSFET 6T SRAM cell using TCAD and compared a conventional structure with partial bottom dielectric isolation.

The source study evaluates alpha particles and heavy ions, multiple strike locations, and hold/read/write conditions. It identifies the drain–channel junction of an off pull-down device as a sensitive region. It also reports that hold operation has the lowest heavy-ion threshold LET among the operating states examined. PDI is intended to limit charge migration from the substrate toward the drain.

Objectives

Explain the SEU mechanism in nanosheet-based 6T SRAM.

Summarize the published TCAD method and findings without presenting them as new results.

Quantify published collected-charge comparisons using transparent arithmetic.

Define a reproducible follow-on study for PDI geometry and strike conditions.

Identify the metrics and limitations required for a credible research submission.

II. Literature Survey (Related Work)

Prior research has examined charge collection in silicon junctions, transient response in SRAM, radiation-hardening structures, and soft-error scaling across planar CMOS, FinFET, and emerging device architectures. The studies below are cited by or closely related to the base paper. Descriptions are concise summaries; consult the full original publications before final submission.

Ref.	Approach / topic	Contribution	Limitation / relevance
[1] Bang et al., 2024	3-nm GAA NSFET 6T SRAM; Sentaurus TCAD; alpha and heavy-ion strikes; conventional vs PDI.	Direct base paper; compares strike location, operation mode, charge collection, and node voltage.	PDI benefit is limited at high LET.
[2] Loubet et al., 2017	Stacked nanosheet GAA transistor technology.	Motivates nanosheet scaling beyond FinFET.	Not an SRAM SEU study by itself.
[3] Narasimham et al., 2021	Soft-error scaling from planar to 5-nm FinFET SRAM.	Shows need to reassess radiation reliability during scaling.	Device platform differs from 3-nm NSFET.
[4] Hsieh et al., 1983	Charge collection from alpha-particle tracks in silicon.	Foundational charge-collection physics.	Older structures and process nodes.

[5] Dodd and Massengill, 2003	SEU mechanisms and modeling in digital microelectronics.	Background for transient generation and upset modeling.	Broad review, not specific to modern nanosheet SRAM.
[6] Elwailly et al., 2021	TCAD radiation-hardness study of FinFET and nanowire SRAM.	Related nanoscale simulation study.	Different device geometry.
[7] Chatterjee et al., 2011	Single-event charge collection in dual-/ triple-well bulk CMOS SRAM.	Illustrates well-isolation approaches.	40-nm bulk results do not directly transfer to 3-nm GAA.

The literature indicates that upset tolerance depends on collected charge, restoring current, storage-node capacitance, strike position, and the particle's energy-deposition profile. Structural isolation can reduce charge collected at a drain, but it may not prevent an upset when deposited charge is sufficiently high.

Fair comparisons require matched device models, bias conditions, particle parameters, and strike coordinates. If PDI thickness and transistor dimensions are both changed in one experiment, the cause of a performance difference becomes ambiguous. A controlled parameter sweep is therefore recommended.

III. Problem Statement and Research Gap

The technical problem is to determine how radiation-generated charge at sensitive regions of a scaled nanosheet SRAM cell perturbs the storage-node voltage and whether a process-level isolation structure reduces that perturbation enough to prevent a bit flip.

During a particle strike, transient charge collection at the drain of an off pull-down transistor can reduce the restoring margin. If the storage-node voltage crosses the inverter's switching region for long enough, the cell may change state. A mitigation method should reduce collected charge, increase the critical charge required for upset, improve recovery, or combine these effects without unacceptable penalties.

Research gap grounded in the base paper

Bang et al. [1] report that PDI reduces collected charge and improves response for lower tested LET values, while the benefit is limited at higher LET where the cell can still flip. This motivates investigating PDI geometry and the conditions under which protection becomes insufficient. This draft does not establish novelty for any specific new geometry; a current literature and patent search is required before claiming novelty.

Research questions

- How does PDI geometry affect collected charge and storage-node voltage for fixed LET and strike location?
- How does the PDI benefit change between hold, read, and write modes?
- What relationship exists between LET, collected charge, and bit-flip occurrence?
- Does a geometry that reduces charge collection introduce unacceptable device or process penalties?

Measurable objectives

Reproduce the published baseline trend before making design changes.

Extract transient voltage, collected charge, recovery time, and upset/no-upset outcome.

Perform a controlled geometry sweep with the device model and strike settings held constant.

Report improvements only from matched simulations, including limitations and uncertainty.

IV. Proposed Methodology and System Architecture

A. Baseline 6T SRAM cell

A standard 6T SRAM bitcell contains two cross-coupled CMOS inverters and two access transistors controlled by the word line (WL). The bit lines BL and BLB are complementary during differential write and read operations. Storage nodes are commonly denoted Q and QB. The base paper labels its internal nodes VCH and VCL and examines the off-state right pull-down transistor.

B. Conventional versus PDI structure

The PDI scheme includes a partial bottom dielectric isolation layer intended to restrict charge migration from the substrate into the drain region. The logical 6T topology is retained; the principal change is to the device/process structure affecting charge collection. Thus, PDI should not be described as an extra SRAM transistor.

C. Follow-on proposed extension (not yet validated)

A feasible extension is a parameterized PDI geometry study. Keep the SRAM topology, calibrated device model, bias conditions, ion-track radius, incident direction, and strike timing constant. Sweep one PDI parameter at a time—for example, dielectric thickness or lateral coverage—over physically justified values supported by the process model. Then repeat selected cases across LET and operating mode. Geometry limits must be confirmed against the TCAD model.

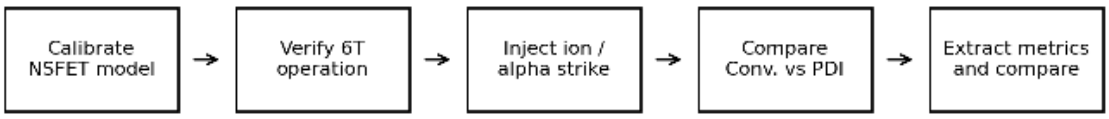


Fig. 1. Proposed reproducible TCAD workflow; this is a methodology diagram, not a simulation output.

D. Algorithmic steps

Calibrate the nanosheet model against a published or measured I–V reference.

Construct the 6T cell and verify operation without radiation.

Set the initial storage state and operation bias.

Inject alpha-particle or heavy-ion charge at a defined location and time.

Record carrier density, transient current, collected charge, and node voltage.

Repeat the same test for the PDI structure with identical settings.

Sweep LET, strike location, operation mode, and proposed geometry.

Determine upset outcome, threshold LET, recovery time, and trade-offs.

IV. Proposed Methodology (continued): Mathematical Model

The following equations define metrics suitable for the study. They do not produce device simulation by themselves; current and voltage waveforms must be extracted from TCAD.

A. Collected charge

The collected charge at a sensitive terminal can be computed by integrating the terminal current over an event window after subtracting the pre-strike baseline current:

$$Q_{col} = \int (I_{terminal}(t) - I_{baseline})\, dt \quad (1)$$

Use the same integration window for conventional and PDI cases. If the simulator provides carrier collection separately from terminal current, document the definition and apply it consistently.

B. Critical charge and upset criterion

Critical charge is the minimum deposited or collected charge that causes the stored state to cross into the opposite stable state under a defined bias and strike condition. It should be obtained through a controlled sweep of deposited charge or LET.

$$Q_{crit} \approx C_{node} \cdot \Delta V_{crit} \quad (2)$$

This is a first-order lumped approximation only. Nonlinear capacitance, transient conduction, and feedback in a nanosheet device require detailed simulation.

C. Threshold LET

$$LET_{th} = \min\{LET : \text{the defined upset criterion is satisfied}\} \quad (3)$$

Threshold LET is conditional on strike location, incident direction, operation mode, bias, and pulse model; it is not a universal device constant.

D. Relative collected-charge reduction

$$\text{Reduction (\%)} = [(Q_{conv} - Q_{PDI}) / Q_{conv}] \times 100 \quad (4)$$

E. Recovery time

$$t_{rec} = t_{return\text{-}to\text{-}tolerance\text{-}band} - t_{strike} \quad (5)$$

Define the voltage tolerance band and the required time for which the node must remain inside it. A transient that briefly returns and then flips should not be counted as successful recovery.

F. Statistical reporting

$$\bar{x} = (1/N) \Sigma x_i ; \quad s = \sqrt{[\Sigma (x_i - \bar{x})^2/(N - 1)]} \quad (6)$$

$$\text{Observed upset fraction} = N_{upset} / N_{trials} \quad (7)$$

A simulated upset fraction is not automatically a field failure rate. Estimating a system-level rate requires a justified radiation environment, event-rate model, and statistical assumptions.

V. Simulation Setup and Experimental Methodology

A. Tool and device-model setup

The base study used Synopsys Sentaurus TCAD to simulate a 3-nm-node GAA nanosheet FET 6T SRAM

cell. The original paper reports calibrated device characteristics and radiation models. A reproduction requires access to an appropriate device model and the full set of geometry, mesh, material, and physical-model parameters; missing parameters should not be guessed.

Parameter	Reported base-paper setup	What to document
Device platform	3-nm-node GAA NSFET	Sheet count, channel dimensions, geometry, model version.
Supply voltage	0.7 V in reported transient examples	Bias waveform and timing per operating mode.
Particle models	Alpha particles and heavy ions	Energy or LET and track-generation settings.
Heavy-ion LET	5, 7, 10 MeV·cm²/mg in charge comparison	Matched LET values for both structures.
Track radius	10-nm Gaussian charge distribution	Track radius and incident direction.
Strike positions	Drain–channel junction, drain extension, drain region	Coordinates and affected device.
Operation	Hold, read, write	Initial state, WL, BL, BLB, and timing.
Isolation	Conventional and PDI	PDI geometry and all parameters changed.

B. Device physics and calibration

The base paper describes field-dependent mobility, inversion/accumulation mobility, unified mobility, Shockley–Read–Hall and Auger recombination, band-to-band tunneling, gate-induced drain leakage, quantum-confinement treatment, bandgap narrowing, and stress/strain effects. A reproduction must report the models actually enabled in the simulation deck rather than assume all are enabled.

C. Validation before radiation testing

Compare NMOS and PMOS transfer curves against calibration references.

Verify hold retention for both logic states.

Verify writeability and read behavior without particle injection.

Refine the mesh near the drain–channel junction and PDI region.

Check time-step convergence around the strike and recovery.

Archive simulator version, model cards, mesh, decks, and extraction scripts.

VI. Results and Discussion

A. Published collected-charge results

The base paper reports the following collected-charge values for conventional and PDI structures under heavy-ion strikes. These are source-paper values and are not simulations generated for this draft.

LET (MeV·cm²/mg)	Conventional (fC)	PDI (fC)	Reduction calculated from source values
5	3.07	2.54	17.26%
7	4.35	3.71	14.71%
10	6.37	5.60	12.09%

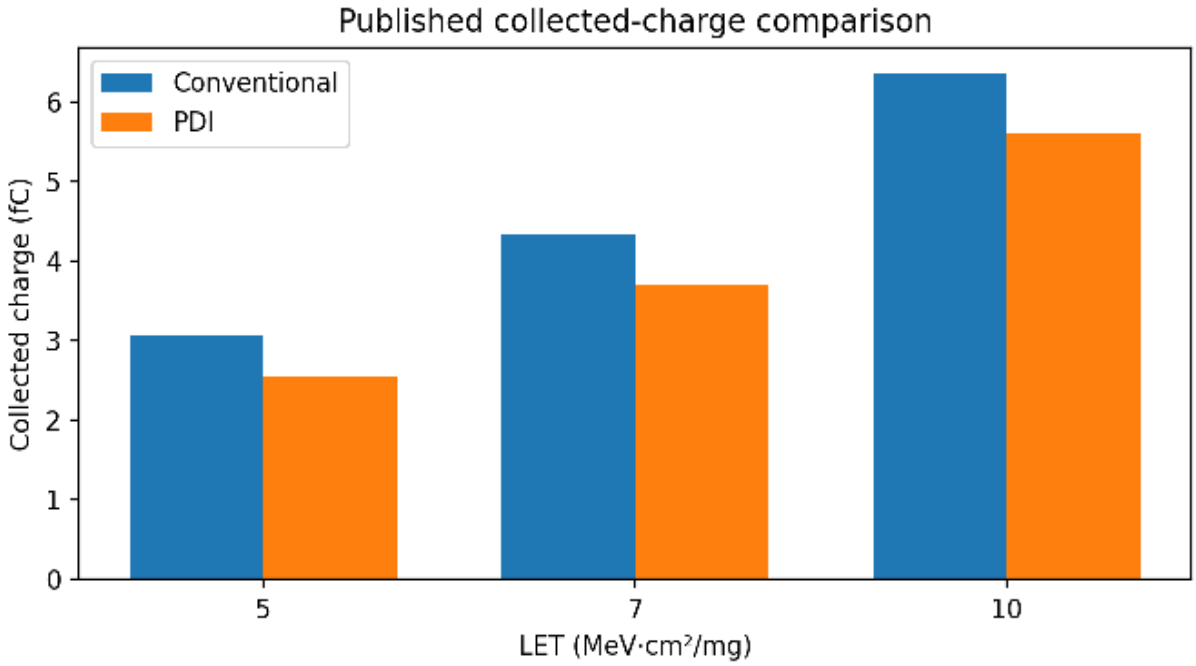


Fig. 2. Published collected-charge comparison from Bang et al. [1]; plotted values are not new simulation results.

PDI has lower collected charge at all three reported LET points. The calculated reduction decreases from about 17.26%at LET 5 to about 12.09%at LET 10. This is consistent with a mitigation mechanism that limits charge collection but does not eliminate the effect of stronger heavy-ion strikes.

VI. Results and Discussion (continued)

B. Published electron-density comparison

For the hold-operation example at LET = 5 MeV·cm²/mg, the base paper reports peak electron density of approximately $3.00 \times 10^{19} cm^{-3}$ in the conventional structure and $5.77 \times 10^{17} cm^{-3}$ in the PDI structure. The logarithmic plot below reproduces these source values.

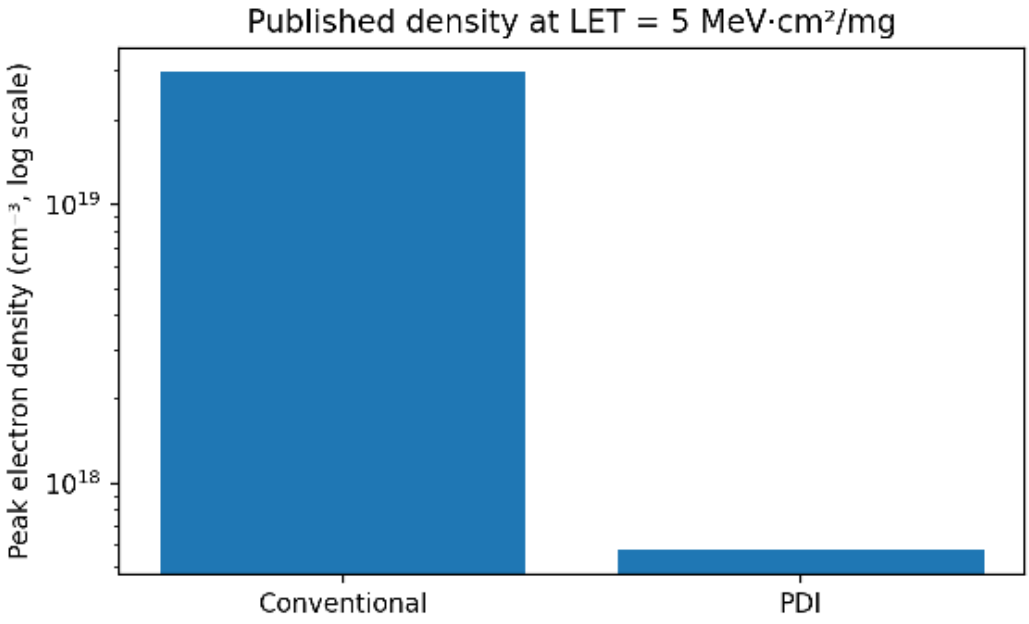


Fig. 3. Published peak electron density at LET = 5 MeV·cm²/mg, reproduced from [1].

$$(3.00 \times 10^{19}) / (5.77 \times 10^{17}) \approx 52.0 \quad (8)$$

The conventional peak density is approximately 52 times the PDI value in this specific reported case. This ratio should not be generalized to all LET values, strike locations, or operating modes. Electron density should be interpreted alongside collected charge and storage-node voltage.

C. Transient response and operating mode

The base paper identifies hold operation as the most vulnerable mode among those tested, with the lowest heavy-ion threshold LET. For the PDI example at LET = 5 MeV·cm²/mg, it reports a voltage drop of approximately −0.21 V at the high storage node in the cited transient case. At higher tested LET values, deposited charge can exceed the restoring capability and a bit flip can still occur.

D. Results required for the proposed extension

Metric	Conventional	PDI baseline	New geometry sweep
Collected charge	Reproduce TCAD	Reproduce TCAD	TBD—run TCAD
Peak node excursion	Extract	Extract	TBD—run TCAD
Recovery time	Extract	Extract	TBD—run TCAD
Threshold LET	Sweep	Sweep	TBD—run TCAD
Upset fraction	Define method	Define method	TBD—run TCAD
Process/area penalty	Baseline	Document	Estimate only if supported

VI. Results and Discussion (continued): Example calculations

A. Charge reduction

For LET = 5 MeV·cm²/mg, the source reports Qconv = 3.07 fC and QPDI = 2.54 fC:

$$[(3.07 - 2.54) / 3.07] \times 100 = 17.26\% \quad (9)$$

For LET = 10 MeV·cm²/mg:

$$[(6.37 - 5.60) / 6.37] \times 100 = 12.09\% \quad (10)$$

These are arithmetic comparisons calculated from published source values, not independently measured performance.

B. Discussion and trade-offs

The evidence supports the claim that PDI lowers collected charge under the tested conditions, not the stronger claim that PDI prevents all SEUs. The follow-on geometry sweep should seek a trade-off between reduced charge collection, nominal SRAM behavior, and fabrication feasibility. Improvements must be demonstrated under matched conditions and across more than one favorable strike location.

VII. Limitations and Reproducibility

- The source study is TCAD-based; it does not report silicon irradiation measurements in the article.
- PDI mitigation is limited at high LET in the tested cases.
- Results depend on geometry, material parameters, track radius, incident angle, and physical models.
- A limited set of strike positions cannot represent all particle trajectories or array-level multi-cell effects.
- Process variability, manufacturing yield, and system-level soft-error rates require separate study.

Reproducibility checklist

- Archive decks, mesh, structure files, model settings, and simulator version.
- Record initial state, bias waveforms, strike time/location, LET, angle, and track radius.
- Use identical conditions for conventional and PDI cases.
- Check mesh/time-step sensitivity and convergence.
- Provide raw extracted data behind each plot.
- Label published, calculated, simulated, and proposed values separately.

VIII. Conclusion

This draft has organized the SEU problem in a 3-nm-node GAA nanosheet FET 6T SRAM cell and summarized the mitigation approach reported by Bang et al. The published study identifies the drain–channel junction of an off pull-down transistor as a sensitive region and finds hold operation particularly vulnerable under the tested heavy-ion conditions. PDI reduces collected charge relative to the conventional structure at LET values of 5, 7, and 10 MeV·cm²/mg; arithmetic reductions calculated from the source values are approximately 17.26%, 14.71%, and 12.09%, respectively. These are calculations from published values, not new simulations.

The source results also show that mitigation is not absolute: at higher LET, the cell can still upset when deposited charge exceeds its restoring capability. A credible extension is a controlled PDI geometry sweep with calibrated device physics, matched strike conditions, mesh/time-step validation, and transparent

extraction of charge, node-voltage excursion, recovery time, and threshold LET. No new optimum or performance gain should be claimed until those simulations are completed.

IX. Future Scope

Sweep physically justified PDI thicknesses and lateral coverage, varying one parameter at a time.
Expand strike-location, incident-angle, and track-radius studies.
Test both stored logic polarities and hold/read/write operation.
Perform process, voltage, temperature, and geometry variation studies.
Compare device-level isolation with circuit-level hardening while accounting for area, power, delay, and writeability.
Extend to SRAM arrays to investigate multi-node charge collection and multi-cell upsets.
Validate TCAD predictions using radiation testing or a calibrated test structure where feasible.
Estimate system-level soft-error rate only with a justified radiation environment and event-rate model.

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